I claim:

1. A method for discovering a connectivity relationship among a plurality of external connections to a two dimensional logic cell, the method comprising the steps of:

   (a) for all contiguous sets of one or more of the external connections, applying a voltage to each contiguous set and measuring a total current flow received by the remainder of the external connections;

   (b) examining a current flow measurement corresponding to a contiguous set of the external connections;

   (c) grouping the contiguous set of external connections if the measured current flow falls below a threshold; and

   (d) repeating steps (b)-(c) for different contiguous sets of external connections.

2. The method of claim 1 wherein each previously grouped set of external connections is treated as a single external connection.

3. The method of claim 1 further comprising the step of using the connection groupings to discover a logical relationship among the external connections.

4. The method of claim 3 wherein the connection groupings are used to generate an ordered binary decision diagram (OBDD).

5. The method of claim 4 wherein the connection groupings comprise a set of variables and orderings on those variables that are used to generate the OBDD.

6. The method of claim 1 wherein the current flow threshold is predetermined.

7. The method of claim 1 wherein the current flow threshold is dynamically determined.

8. The method of claim 1 wherein the logic cell is a nanocell.

9. The method of claim 8 wherein the nanocell is a regular polygon.

10. The method of claim 9 wherein the regular polygonal nanocell is further characterized by one or more external connections on one or more sides of the polygon.

11. The method of claim 9 wherein each side of the polygonal nanocell has at least one external connection.

12. The method of claim 9 wherein the nanocell has at least 20 external connections.

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1   13. The method of claim 9 wherein the nanocell has at least 4 external connections.

1   14. The method of claim 9 wherein the nanocell includes an assembly of nanocells which

2   are of one or more planar geometries.

1   15. The method of claim 14 wherein discovery of connectivity relationships is at least

2   partially effected by or through neighboring nanocells.

1   16. A method for discovering a connectivity relationship among a plurality of external

2   connections to a two dimensional logic cell, the method comprising the steps of:

3   (a) applying a voltage to a contiguous set of one or more of the external

4   connections;

5   (b) measuring a total current flow received by the remainder of the external

6   connections;

7   (c) grouping the contiguous set of external connections if the measured current

8   flow falls below a threshold; and

9   (d) repeating steps (a) – (c) for different contiguous sets of external connections.

1   17. A method for programming a series of interconnected devices, wherein each device is

2   capable of assuming at least two stable states, the devices initially being in a first

3   state, the method comprising the step of:

4   applying a voltage pulse to an input to the devices, the voltage pulse having a

5   first polarity and a time duration sufficient to cause a number x of devices to

6   switch to a second state.

1   18. The method of claim 17 further comprising the step of applying a second voltage

2   pulse to the input, the second pulse having a second polarity and a duration sufficient

3   to cause a number y of devices to return to the first state, where y is less than x.

1   19. The method of claim 18 further comprising the step of applying subsequent voltage

2   pulses to the input, the subsequent voltage pulses having alternating polarity and

3   progressively shorter duration.

1   20. The method of claim 19 wherein the numbers x and y are predetermined.

1   21. The method of claim 19 wherein the numbers x and y are dynamically determined.

1   22. The method of claim 17 wherein the interconnected devices are molecular switches

2   having a characteristic negative differential resistance.

1   23. The method of claim 17 wherein the logic cell includes switching devices of different

2   switching potentials.

1   24. The method of claim 17 further including the step of devices assuming a known state

2   at some time subsequent to the application of the first pulse.

1   25. The method of claim 17 wherein the interconnected device are molecular switches

2   within nanocells, and wherein logic cell programming is at least partially effected by

3   or through neighboring nanocells.

1   26. A method for re-programming a series of interconnected devices, wherein each

2   device is capable of assuming at least two stable states, the devices initially being in

3   an operational state, the method comprising the step of:

4   applying a voltage pulse to an input to the devices, the voltage pulse having a first

5   polarity and a time duration sufficient to cause a number x of devices to switch to a

6   second state.

1   27. A method for programming a logic cell having a plurality of external connections

2   interconnected by a plurality of switching devices, the method comprising the steps

3   of:

4   (a) discovering a logical relationship among the external connections to the logic

5   cell;

6   (b) programming the switchable devices to perform a logic function by using a

7   series of voltage pulses having alternating polarity and progressively shorter

8   duration;

9   (c) testing the logic cell to determine if it performs the programmed logic

10   function;

11   (d) repeating steps (a)-(c) as necessary to ensure the logic cell performs the

12   programmed logic function.

1   28. A method for programming a logic cell having a plurality of external connections

2   interconnected by a plurality of switching devices, the method comprising the steps

3   of:

4   (a) discovering a logical relationship among the external connections to the logic

5   cell;

6   (b) programming the switchable devices to perform a logic function by using a

7   series of voltage pulses having alternating polarity and progressively shorter

8   duration, where the sequence of duration, voltages and choice of inputs on

9   which to signal those sequences of voltages is chosen based on a logical

10   representation of connectivity within the logic cell;

11   (c) testing the logic cell to determine if it performs the programmed logic

12   function.

1   29. The method of claim 28 wherein the logic cell comprises one or more nanocells.

1   30. A method of re-programming, modifying or repairing a logic cell having a plurality

2   of external connections interconnected by a plurality of switching devices, the method

3   comprising the steps of:

4   (a) determining the operable function of the logic cell;

5   (b) re-programming the switchable devices to perform a selected logic function by

6   using a series of voltage pulses having alternating polarity and progressively

7   shorter duration;

8   (c) confirming operability of the programmed logic cell.

1   31. The method of claim 30 further characterized by performance of the steps after and

2   during such time as the logic cell has commenced an operational mode.

1   32. The method of claim 30 wherein the voltage pulses are selected so as to

2   preferentially influence a subset of the switching device types according to the

3   threshold potential of that subset

1.   33. A method of re-programming, modifying or repairing a logic cell, including the case

2   where such logic cell is a nanocell, such logic cell having a plurality of external

3   connections interconnected by a plurality of switching devices, the method

4   comprising the steps of:

5   (a) determining the operable function of the logic cell;

6   (b) re-programming the switchable devices to perform a selected logic function by

7   using a series of voltage pulses having alternating polarity and progressively

8   shorter duration, and where the sequence of duration, voltages and choice of

9   inputs on which to signal those sequences of voltages is chosen based on a logical

10   representation of connectivity within the logic cell;

11   (c) confirming operability of the programmed logic cell.

1   34. The method of claim 33 further characterized by performance of the steps after and

2   during such time as the logic cell has commenced an operational mode.

1   35. The method of claim 33 wherein the voltage pulses are selected so as to

2   preferentially influence a subset of the switching device types according to the

3   threshold potential of that subset.

1   36. A device containing at least one logic cell programmed by the method of claim 16

1   37. A device containing at least one logic cell programmed by the method of claim 17.

1   38. A device containing at least one logic cell programmed by the method of claim 26.

1   39. A device containing at least one logic cell programmed by the method of claim 27.

1   40. A device containing at least one logic cell programmed by the method of claim 28.

1   41. A device containing at least one logic cell programmed by the method of claim 29

1   42. A device containing at least one logic cell programmed by the method of claim 30.

1   43. A device containing at least one logic cell programmed by the method of claim 33.